

## Overview

Technovare Systems, Inc. offers deep sub-micron ASIC, FPGA, and Embedded System Design Services. With expertise in Logic Design, Verification, Design for Testability (DFT), Circuit Design, and Physical Design, Technovare is well equipped to meet all your ASIC design requirements.



## Logic Design and Verification

- Architecture definition/partition and RTL coding in Verilog/VHDL
- Verification using the latest tools such as Verilog-XL, VCS, Verilog- NC, Modelsim, etc.
- System verification using C++/SystemVerilog/OVM/UVM/VMM, etc.
- IP integration and verification using industry standard bus interfaces
- Creation and verification of Bus Functional Models
- Formal verification and assertion based verification

## Timing Closure and Timing Analysis

- Timing closure using the industry standard synthesis tools
- Static timing analysis to avoid any violations after the synthesis
- Scripting using tcl language and creating a synthesis environment
- Integration with physical synthesis tools

## Design for Testability

- Scan insertion using full, parallel, and partial scan methodology
- BIST controller for testing the embedded memory blocks
- JTAG controller for debugging the boundaries and for debugging the software
- ATPG vectors generation for testing the manufacturing defects

## Physical Design and Verification

- Physical synthesis and Floor planning
- DRC and LVS to check integrity of the design
- Clock skew management and signal integrity issues
- Timing closure and post-layout simulation
- Verifying sub-nano physical design issues
- Get the chip ready for tape out to the foundry
- Tools: Magma, Cadence, Synopsys

## Mixed Signal, Analog, and RFIC

- RF Integration
- High speed SerDes design
- Circuit design and spice simulations
- Embedded Memories: SDRAM, DDR2, DDR3, QDR, etc.
- PLL/DLL, High Speed IO, ADC, DAC

## Silicon Validation & Board Bring Up

- ASIC/FPGA chip Bring Up in lab
- Board level silicon validation & debugging
- Firmware development & debugging
- Turnkey ASIC Design, Packaging, Test, and Production